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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,392	HADIZAD, PEYMAN	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-13 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Blanchard (U.S. Patent 6,686,244).

In re claim 1, **Blanchard** discloses a method of making a semiconductor vertical trench gate junction FET device comprising the steps of:

providing a body of semiconductor material **501** comprising a first conductivity type (n-type), wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact **D** (col. 4, lines 57-64 and FIG. 5(a));

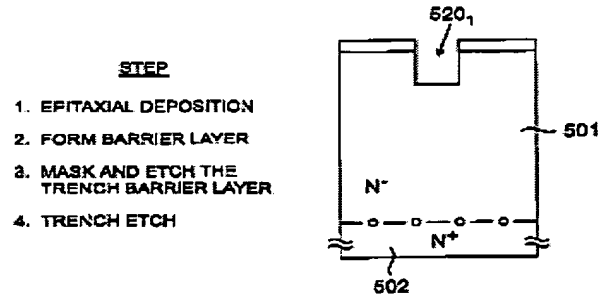


FIG. 5(a)

forming a first trench **520_1** in the body of semiconductor material **501** and extending from the upper surface, wherein the first trench **520_1** has a first width **(unlabeled)**, a first depth **(unlabeled)** from the upper surface, first sidewalls **(unlabeled)**, and a first bottom surface **(unlabeled)** (col. 4, lines 64-65 and FIG. 5(b));

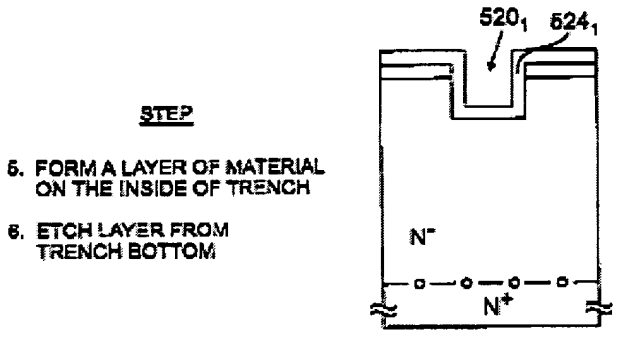


FIG. 5(b)

forming a second trench **520_4** trench within the first trench **520_1** wherein the second trench has a second width **(unlabeled)**, a second depth **(unlabeled)** from the first surface, second sidewalls **(unlabeled)** and a second bottom surface **(unlabeled)** (col. 5, lines 30-40 and FIG. 5(d));

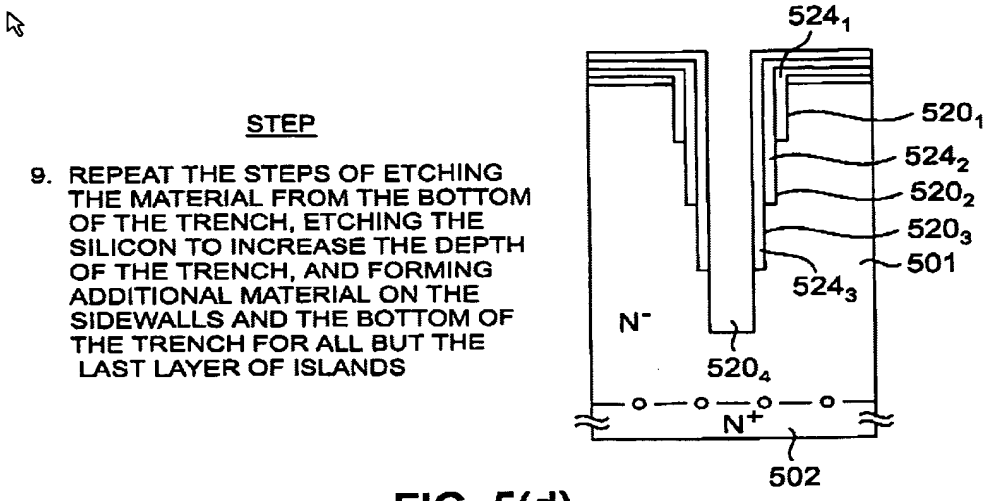


FIG. 5(d)

forming a first source region in the body of semiconductor material **501** extending from the upper surface and spaced apart from the first trench $\mathbf{520_1}$ by a portion of the body of semiconductor material; introducing (IMPLANT) $\mathbf{524_3}$ a dopant (Boron) of a second conductivity type (p-type) into at least a portion of the second sidewalls and the second bottom surface to form a doped trench gate region $\mathbf{550_4}$ wherein the doped trench gate region extends into the body of the semiconductor material for controlling conduction in the device (col. 5, line 60 to col. 6, line 6 and FIG. 5(f));

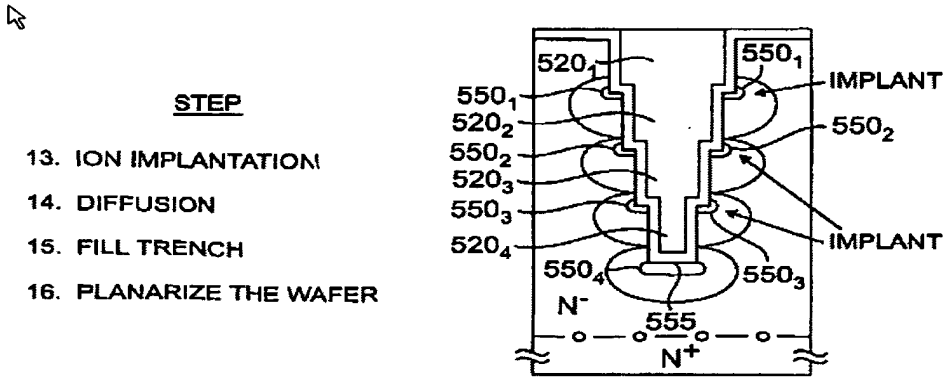


FIG. 5(f)

forming a first passivation layer **540** over the doped gate region $\mathbf{550_4}$ (col. 4, lines 50-57); and forming a second passivation layer (SiO) over the first passivation layer thereby filling at least the second trench $\mathbf{520_4}$ (col. 6, lines 7-14).

In re claim 2, **Blanchard** discloses that the step of providing the body of semiconductor material comprises providing a III-V semiconductor substrate **502** having a first dopant concentration and a first epitaxial layer **501** formed on a surface of the semiconductor substrate, wherein the first epitaxial layer has a second dopant concentration (N-type doped) less than the first dopant concentration (N+ doped) (col. 4, lines 57-64).

In re claim 3, the step of providing a body of semiconductor material comprising GaAs (gallium arsenide) is well-known to one of ordinary skill in the art at the time of the invention was made.

In re claim 4, **Blanchard** discloses that the step of forming the second trench **520_4** comprises the steps of: depositing a spacer layer **524_1** over the upper surface and the first trench **520_1**; etching back the spacer layer to form spacers that cover first sidewalls and a portion of the first bottom surface leaving a self-aligned opening in the spacer layer to expose a remaining portion of the bottom surface; and etching the second trench through the opening (FIGS. 5(b) and 5(d)).

In re claim 5, **Blanchard** discloses that the step of introducing the dopant of the second conductivity type comprises implanting the dopant into the second sidewalls and the second bottom surface (col. 5, line 60 to col. 6, line 7 and FIG. 5(f)).

In re claim 6, the step of implanting the dopant species includes implanting one of beryllium and carbon is well-known to one of ordinary skill in the art at the time of the invention was made.

In re claim 8, **Blanchard** discloses that the step of forming the second passivation comprises the steps of: depositing a dielectric material (SiO) over the first passivation layer **540**; and planarizing the dielectric material to form the second passivation layer (col. 6, lines 7-14 and FIG. 5(f)).

In re claim 9, **Blanchard** discloses that the method of claim 1 further comprising the step forming a second source region in the body of semiconductor material spaced

apart from the first trench by another portion of the body of semiconductor material, wherein the first trench is between the first and the second sources (FIG. 5(b)).

In re claim 10, **Blanchard** discloses that the step of forming the first trench **520_1** includes etching the first trench using one of reactive ion etching (RIE) and electron cyclotron resonance etching (col. 4, lines 64-65).

In re claim 11, **Blanchard** discloses that the step of forming the second trench includes etching the second trench using one of reactive ion etching and electron cyclotron resonance etching (col. 5, lines 30-40).

In re claim 12, **Blanchard** discloses a process of making a compound semiconductor vertical trench gate junction FET device comprising the steps of: forming a first groove **520_1** in a compound semiconductor layer **501** of a first conductivity type (n-type), wherein the first groove has first sidewalls (unlabeled), and a first lower surface (unlabeled), and wherein the first groove extends from a first surface of the compound semiconductor layer (col. 4, lines 57-64 and FIG. 5(a));

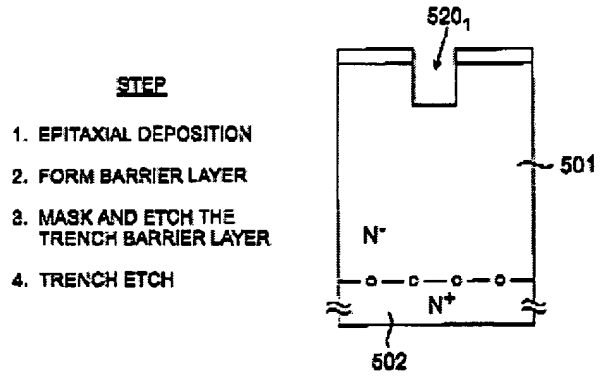


FIG. 5(a)

forming a second groove **520_4** within the first groove **520_1** wherein the second groove has second sidewalls and a second lower surface (col. 5, lines 30-40 and FIG. 5(d));

STEP

9. REPEAT THE STEPS OF ETCHING THE MATERIAL FROM THE BOTTOM OF THE TRENCH, ETCHING THE SILICON TO INCREASE THE DEPTH OF THE TRENCH, AND FORMING ADDITIONAL MATERIAL ON THE SIDEWALLS AND THE BOTTOM OF THE TRENCH FOR ALL BUT THE LAST LAYER OF ISLANDS

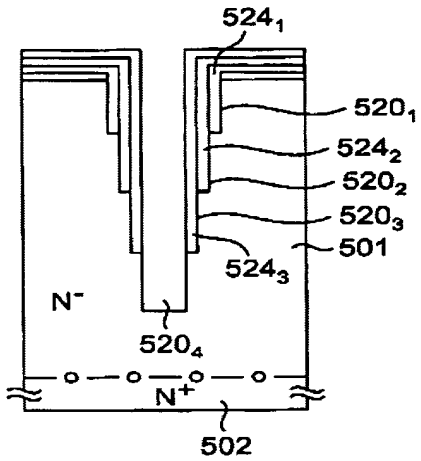


FIG. 5(d)

doping (IMPLANT) the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant (p-type) to form a doped trench gate region **550_4** in the compound semiconductor layer for controlling conduction in the device (col. 5, line 60 to col. 6, line 6 and FIG. 5(f));

STEP

13. ION IMPLANTATION
14. DIFFUSION
15. FILL TRENCH
16. PLANARIZE THE WAFER

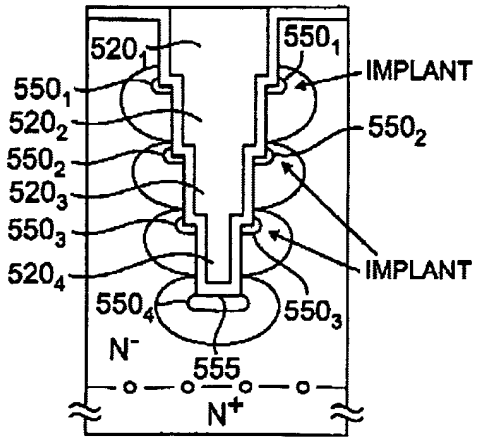


FIG. 5(f)

forming a first source region of the first conductivity type (n-type) in the compound semiconductor layer adjacent to the first groove **520_1** (FIG. (5b));

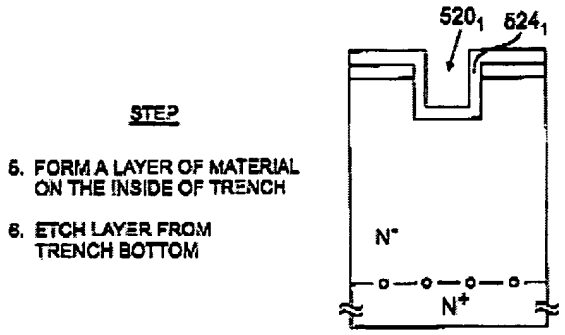
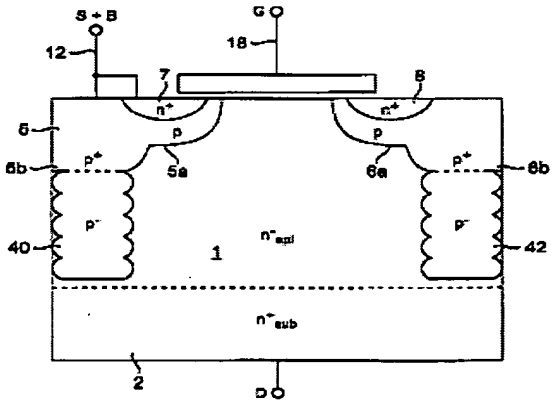


FIG. 5(b)

forming a source contact **12** to the first source region **7**; filling the second groove and at least a portion of the first groove with a passivation layer **540** (col. 6, lines 7-14);

forming a gate contact **18** coupled to the doped trench gate region **550_4**; and forming a drain contact **D** on a second surface of the compound semiconductor layer (FIG. 3);



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 3

In re claim 13, the step of forming the first groove includes forming the first groove in a compound semiconductor layer comprising one of GaAs (gallium arsenide) and InP is well-known to one of ordinary skill in the art at the time of the invention was made (col. 5, lines 12-33 and FIG. 3A).

In re claim 15, **Blanchard** discloses that the step of doping the second lower surface and at least a portion of the second sidewalls includes ion implanting a second conductivity type dopant species Boron (p-type) (col. 5, line 60 to col. 6, line 6).

In re claim 16, **Blanchard** discloses that the step of forming the second groove **520_4** comprises the steps of: forming spacers on the first sidewalls leaving an opening **520** over the first lower surface; and etching the second groove **520_4** in the compound semiconductor through the opening (FIGS. 5(b) and 5(d)).

In re claim 17, **Blanchard** discloses that the steps of forming the first **520_1** and second **520_4** grooves including forming first and second grooves having substantially straight sidewall surfaces (FIGS. 5(b) and 5(d)).

In re claim 18, **Blanchard** discloses a method for forming a compound semiconductor trench gate junction FET device comprising the steps of:

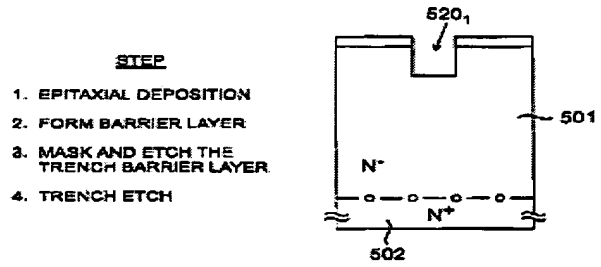
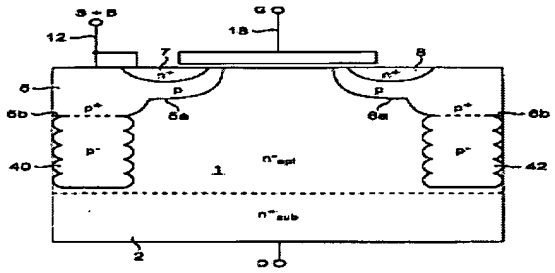


FIG. 5(a)

providing a body **501** of compound semiconductor material including a support wafer **502** of a first conductivity type (n-type) and a first dopant level (N+ doped) and an epitaxial layer **501** formed over the support wafer **502**, wherein the epitaxial layer is of the first conductivity type (n-type) and has a second dopant level (N-type) lower than the first dopant level (col. 4, lines 57-64 and FIG. 5(a));

forming a plurality of spaced apart first doped regions **7, 8** of the first conductivity type (n-type) in the epitaxial layer (FIG. 3);



THE DOPANT DISTRIBUTION OF A HIGH VOLTAGE VERTICAL DMOS TRANSISTOR WITH A RELATIVELY LOW ON-RESISTANCE

FIG. 3

forming a plurality of first trenches 520_1 in the epitaxial layer **501**, wherein each first trench 520_1 is between a pair of first doped regions **7, 8**;

forming a plurality of second trenches 520_4 in the epitaxial layer **501**, wherein one second trench is within one first trench (FIG. 5(d));

STEP

9. REPEAT THE STEPS OF ETCHING THE MATERIAL FROM THE BOTTOM OF THE TRENCH, ETCHING THE SILICON TO INCREASE THE DEPTH OF THE TRENCH, AND FORMING ADDITIONAL MATERIAL ON THE SIDEWALLS AND THE BOTTOM OF THE TRENCH FOR ALL BUT THE LAST LAYER OF ISLANDS

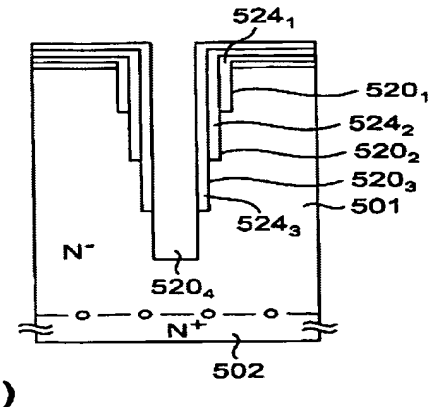


FIG. 5(d)

doping (IMPLANT) at least portions of sidewall surfaces and lower surfaces of each second trench to form a plurality of doped trench gate regions **550_4**, wherein the plurality of doped gate regions extend into the body of compound semiconductor material and are configured for controlling current conduction in the device (col. 5, line 60 to col. 6, line 6 and FIG. 5(f));

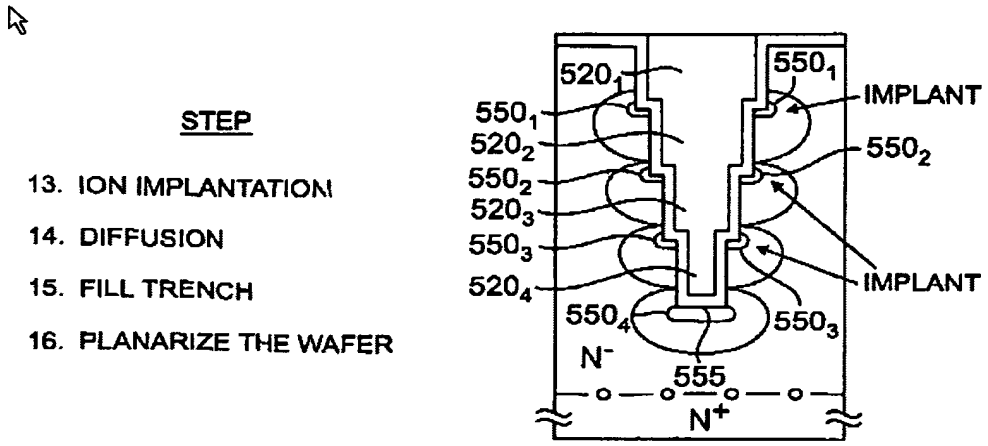


FIG. 5(f)

filling the plurality of second trenches **520_4** and at least a portion of the plurality of first trenches with a passivation material **540** (col.6, lines 7-14);

coupling the plurality of spaced apart first doped regions **7, 8** with a first contact layer; coupling the plurality of doped trench gate regions to a gate **18** connecting region formed in the body of compound semiconductor mateial; and forming a drain contact **D** on a lower surface of the support wafer (FIG. 3);

In re claim 19, the process of providing the body of compound semiconductor material includes providing a body of compound semiconductor material comprising one of GaAs (gallium arsenide) and InP is well-known to one of ordinary skill in the art at the time of the invention was made.

In re claim 20, **Blanchard** discloses that the step of doping the sidewall surfaces and lower surfaces includes ion implanting a dopant of the second conductivity type dopant species (n-type) (col. 5, line 60 to col. 6, line 6).

Response to Applicant's Amendment and Arguments

Applicant's arguments with respect to claims 1-6, 8-13 and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contends that neither reference, Blanchard et al. (U.S. Patent 7,750,104) and Blanchard (U.S. patent 4,914,058) herein known as Blanchard A and Blanchard B, either singularly or in combination, shows or suggests a vertical trench gate junction FET device where the gate region is formed by introducing dopant through the sidewalls and bottom surface of a second trench region, and where the gate region extends into a body of semiconductor material.

In response to Applicant's contention that neither reference, Blanchard A or Blanchard B, either singularly or in combination, shows or suggests a vertical trench gate junction FET device where the gate region is formed by introducing dopant through the sidewalls and bottom surface of a second trench region, and where the gate region extends into a body of semiconductor material. Examiner respectfully submits that Applicant's argument is moot in view of the newly discovered reference to Blanchard (U.S. patent 6,686,244) applied under 35 U.S.C. 102(e) rejection presented in this Office Action. Applicant is directed to (col. 5, line 60 to col. 6, line 6 and FIG. 5(f)) where Blanchard '244 discloses introducing (IMPLANT) **524_3** a dopant (Boron) of a second conductivity type (p-type) into at least a portion of the second sidewalls and the second

bottom surface to form a doped trench gate region **550_4** wherein the doped trench gate region extends into the body of the semiconductor material for controlling conduction in the device.

For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
January 04, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER